A Fractional PLL for the Receiver of DRM Digital Broadcast System

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Abstract—A prototype Fractional PLL was designed to provide LO signal for the receiver of digital broadcast system DRM30. The multi-frequency carriers have a minimum spacing of 41Hz and the receiver LO signal need to have a spectral purity <4Hz to decode the 64QAM modulation. CMOS differential current mode logic was used in the PLL implementation. Using an external crystal oscillator and VCO, and loop BW set to 500Hz, the PLL loop can be programmed with 2 Hz step @ 30MHz LO output and the spectrum purity is < +/-3Hz. The PLL functions at VCC>2V.

Keywords-component; PLL, Frequency Synthesizer, DRM Digital Broadcast, Digital Radio Tuner/Receiver

I. INTRODUCTION

Digital Radio Mondial (DRM30) is a digital broadcast system specified by EBU in 2002 [1] to replace the analog broadcast system in the LW/MW/SW (150KHz-30MHz) radio bands . The system provides a FM quality audio service plus the benefit of digital information and still picture broadcast at the background, as well as the RDS/AMSS functionality. OFDM technique is used and the modulation bandwidth the same as the traditional AM channel bandwidth (5/10 KHz).

The proposed system provides a challenge for the design of the radio frequency tuner. Within the frequency bandwidth, there will be allocated 288 carriers, the minimum spacing between neighboring carriers is about 41Hz. It is required that the channel programming step to be 1KHz. However, a finer frequency programming step would be beneficial that LO signal could be adjusted to match the incoming carrier.

A design exercise had been carried out to implement a Fractional PLL using the CMOS devices of a 0.6um BiCMOS process. Differential current mode logic [2] is used for the prescaler, reference counter and phase detector circuits. The low Vds drop in active mode for the CMOS devices enable the circuit to function at VCC>2V (instead of 2.7V for Bipolar circuit). The reduced voltage swing of the differential logic enables the logic gates to function at 2-3 times that of the traditional CMOS logic gates, with the penalty of constant current passing through the logic gates.

The prescaler funtions up to 250MHz and divided down to provide <30MHz DRM LO quadrature signals.

A traditional Integer PLL [2,3,4] is modified so that the prescaler division ratio N could be switched between N/N=1 or N/N+2 at the phase comparison frequency. The PLL itself functions as a low pass filter for the division ratio, so that the effective division ratio is the time average of the div(N/N+1) ratio. A frequency step of ~20Hz can be programmed at the VCO output (@ 240MHz), this is equivalent to a programmable step of ~3Hz at the LO output (@30MHz).

Using external XO and VCO units with good phase noise performance in the PLL, the LO signal output could have a spectral resolution of < +/-3Hz.

II. SYSTEM SIMULATION STUDY

A. *Spectral Resolution required for decoding 64QAM*

A simulation had been carried out in MatLab to study the effect of frequency jitter and drift of the LO signal on the distortion of the constellation points of the received DRM symbol. The effect is modeled by the accumulated phase shift introduced by a random fluctuation of frequency at each time point of the symbol period (within +/-Δf limit)and a linear drift of f_drift. After the OFDM demodulation (a FFT process), the constellation points are scattered in the I/Q diagram. Figure 1a shows the results obtained over 10 symbols with Δf=4Hz and f_drift=4Hz/sec. Figure 1b shows the results with Δf=10Hz and f_drift=4Hz/sec. Figure 1c shows the results with Δf=15Hz f_drift=4Hz. Figure 1d shows the results with Δf=0Hz, drift =82Hz.

The effect of LO frequency drift is a rotation of the phasor diagram of the constellation points. This effect could always be corrected by the demodulation software as each DRM symbol content frequency reference carriers and the frequency drift can be estimated for each symbol and compensated for by an angle rotation routine. The major distortion is caused by the frequency jitter and this results in the constellation points to be close to each other and lead to uncertainty in decoding. A good receiver should have a LO frequency jitter < 4Hz.

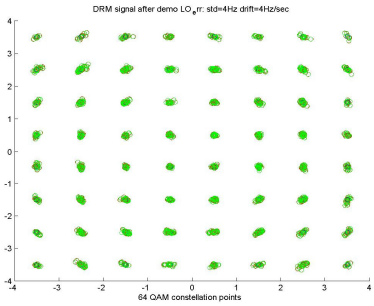

Fig 1a

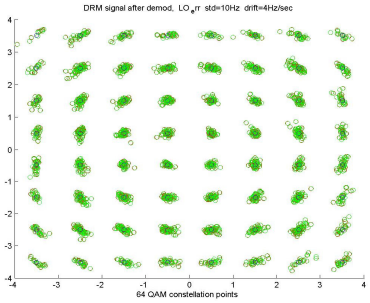

Fig. 1b

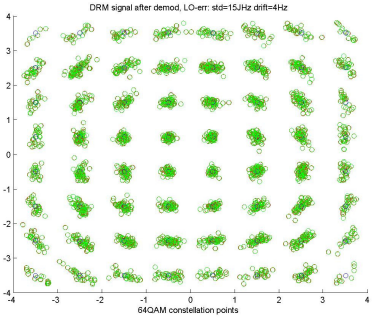

Fig. 1c

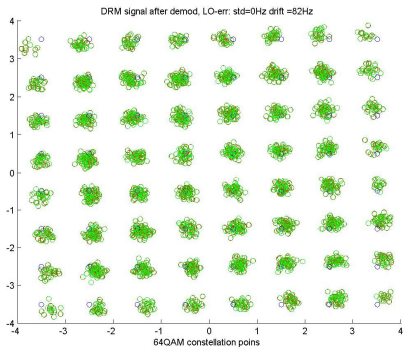

Fig. 1d

B. Frequency Resolution and Programmability Study of Fracitonal PLL Algorithm

A traditional integer PLL was modified so that the prescaler division ratio could be switched between 2 neighboring integer values of N/N+1 or N/N+2. The switching is controlled by a 3rd order Delta-Sigma modulator [5,6,7]. The PLL loop filters out the high frequency switching noise from the VCO control voltage, and the prescaler achieves a time averaged division ratio between N/N+1 or between N/N+2. The relationship between the PLL loop bandwidth and the resolution of the fractional division ratio / frequency error is studied in the MatLab environment . Fig. 3 shows the PLL loop lock-in response during a change of frequency, and each curve represent the response of a different loop bandwidth. One of the response (green) is that of a critical damping condition – optimum between lock-in time and the frequency error. The results show that at a loop bandwidth of ~200 Hz, the VCO output has a frequency error of <15Hz_pp @ 260MHz. This converts to <2Hz_pp at the LO output @ 30MHz, PLL lock-in time~100ms.

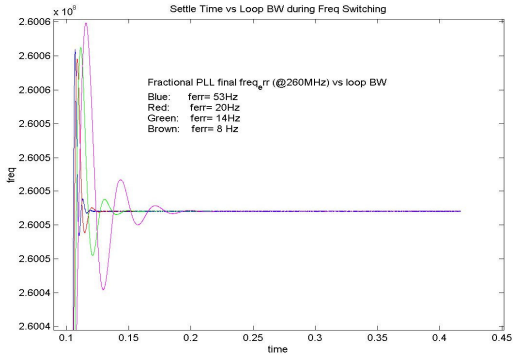

Fig.2

TABLE I. PLL SIMULATION

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PLL simulation performance		
Loop bandwidth	f_err_pp @ 260MHz	Lock-in time
400Hz	57Hz	35ms
280Hz	28Hz	50ms
200Hz	15Hz	100ms
140Hz	8Hz	150ms

III. IMPLEMENTATION OF THE PLL

The CMOS devices in a 0.6um BiCMOS process was used for the implementation of the Fractional PLL. The 4mm*3mm chip has the following on chip blocks (Fig.4) : prescaler, reference counter, phase detector and charge pump, Delta-Sigma modulator and control logic. External crystal oscillator and VCO are used to give a better phase noise performance.

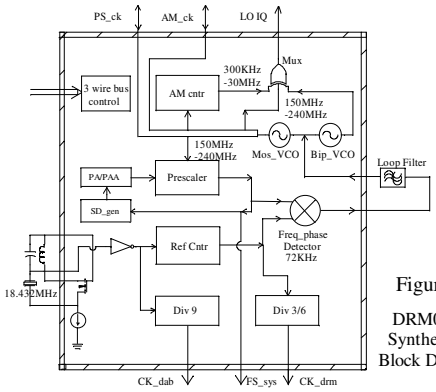

Figure 1
DRM002 Synthesiser Block Diagram

Fig. 4

The prescaler and reference counter are designed using differential current mode logic (Fig 5) instead of the traditional CMOS logic. This is a tradeoff between DC current and supply voltage headroom, phase noise and speed. CMOS devices had a lower Vds in active region in compare with the Vbc of Bipolar devices, this enables the CMOS CML logic to function @Vcc>=2V instead of 2.7V for the Bipolar part.

A differential charge pump is used so that a reasonable control voltage range of 0.5-1.5V (between CAP1 and CAP2 ports) can be applied to the VCO control. The differential charge pump arrangement reduces the effect of Vcc pulling. The average of the 2 output ports are maintained by feedback to bias voltage BSRef. Current sourced and sinked to the CAP1 and CAP2 ports match each other, so that no charging current between the CAP1 and CAP2 ports unless there is a mismatch of input current between PD1 and PD2 ports.

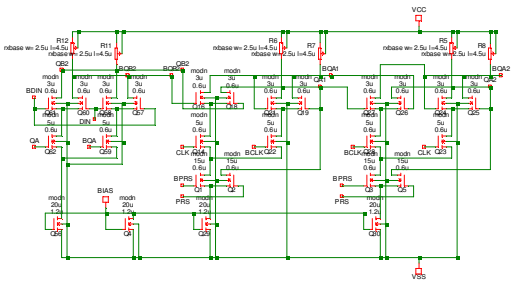

Fig. 5 CMOS CML logic

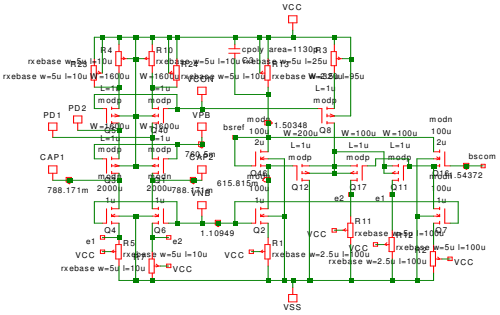

Fig 6 Differential Charge Pump

IV. MEASUREMENT RESULT

The PLL functions with Vcc>=2V. The VCO output spectrum @200MHz with a loop bandwidth of ~500Hz is shown in Fig. 6. Probably due to the higher noise floor in the charge pump, PLL loop in band noise floor is high, only 20-25dB below the signal peak (Fig. 7). After frequency division down to the LO signal output @ <20MHz region, the in band noise floor is below 70dB of the signal peak, and the LO signal has a spectral bandwidth <3Hz (Fig.8). This is similar to the XO reference signal spectral bandwidth .

Fig. 7 Spectrum of PLL output @VCO buffer
Spectrum analyser setting:
BW=1Hz, SPAN=100Hz

Fig. 8 Spectrum of PLL output @LO port
Spectrum analyser setting:
BW=1Hz, SPAN=30Hz

In the Fractional Synthesize mode, the VCO signal could be programmable by 20Hz step (Fig.9a/b/c). This translates into a programmability of ~2Hz step at the LO signal.

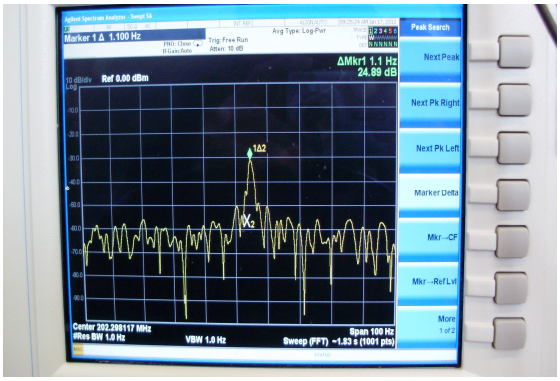

Fig. 9a PLL fractional frequency operation
f_c= 200MHz, SPAN=100Hz, RES=1Hz

Fig. 9b PLL fractional frequency operation
f_c= 200MHz+Δf, SPAN=100Hz, RES=1Hz

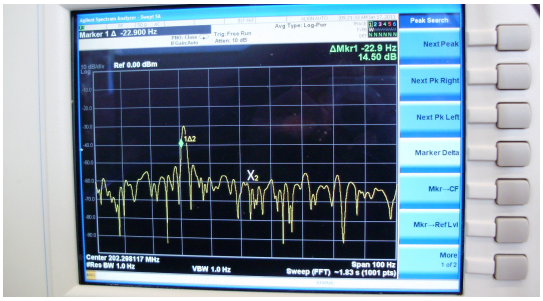

Fig. 9c PLL fractional frequency operation
f_c= 200MHz-Δf, SPAN=100Hz, RES=1Hz

There is a frequency drift of ~10-20Hz @ the VCO signal in the measurement setup caused by the instability of the XO oscillation. The frequency drift could be reduced if a signal source of better stability is used.

The performance of the PLL circuit is summarized in the following table:

TABLE II.

PLL performance for DRM30		
Parameter	***Target***	***Proto-type***
DC supply voltage	2V	>2V
Current consumption		25ma
Loop bandwidth	200Hz	500Hz
VCO spectral resolution	15Hz_pp	15Hz
LO spectral resolution	2Hz_pp	<+/-3Hz
VCO noise floor	<-40dB	20-25dB
LO noise floor		<-70dB
Lock in time	100ms	

V. SUMMARY

A Fractional PLL circuit had been designed. A 3rd order single bit Δ-Σ modulator is used to control the fractional division ratio of the prescaler so that a fine step of 20Hz can be achieved at the VCO port (170-250MHz) . After dividing down to under 30MHz, the fine step of ~2Hz and spectral resolution of ~+/-3Hz can be obtained at the LO quadrature ports. The prescaler, reference couter, phase detector and AM counter, Δ-Σ modulator and control logic are designed in CMOS devices in a 0.6um BiCMOS process. The VCO and crystal oscillator are external bipolar devices in this prototype implementation. The PLL is suitable to be used in the LO frequency synthesizer of a DRM30 digital radio receiver.

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